We Claim:

1. A method for collecting memory failure information in real time while performing a test of memory embedded in a circuit, comprising:

for each column or row of a memory under test:

testing each memory location of said column or row according to a memory test algorithm under control of a first clock;

selectively generating a failure summary on-circuit while performing said testing; and

transferring said failure summary from said circuit under control of a second clock concurrently with testing of the next column or row in sequence.

2. A method as defined in claim **1**, further including initiating said transferring said failure summary at the end of testing said column or row or at the end of transferring of an immediately preceding failure summary.

3. A method as defined in claim **2**, further including delaying testing of a second next column or row in sequence until said failure summary has been completely transferred off-circuit.

4. A method as defined in claim **1**, further including performing said transferring said failure summary during a transfer time substantially equal to the time required to test a corresponding row or column.

5. A method as defined in claim **4**, said failure summary having a bit length equal to or less said transfer time divided by the period of said second clock.

6. A method as defined in claim **5**, said generating a failure summary including generating a column failure summary having a first set of fields when said memory is accessed in column access mode, generating a row failure summary having a second set of fields when said memory is accessed in row access mode, and a phase failure summary having a third set of fields upon completion of a test phase.

7. A method as defined in claim **1**, further including performing said transferring said failure summary during a transfer time equal to or less than the time required to test corresponding row or column.

8. A method as defined in claim **1**, each said failure summary comprising a combination of one or more of a column or row failure address, one or more failure counts, and failure mask data.

9. A method as defined in claim **8**, said failure mask data being results of comparisons between memory data outputs and expected memory data outputs.

10. A method as defined in claim **1**, said generating a failure summary further including classifying each detected failure according to predetermined failure types, maintaining a count of the number of failures of each of said predetermined failure types and including a count of each said failure types in said failure summary.

11. A method as defined in claim **10**, said predetermined failure types including a massive failure type indicative of a predetermined number of failures in adjacent locations in a word of said memory.

12. A method as defined in claim **10**, said predetermined failure types including a non-massive failure type including a single bit failure type and a multi-bit failure type.

13. A method as defined in claim **12**, said failure summary including the row or column address of each of first and last failures detected in said column or row, respectively, and a count of each said predetermined failure types.

14. A method as defined in claim **8**, said step of generating a failure summary including selecting failure summary content based on memory test phase and/or memory access mode.

15. A method as defined in claim **1**, said generating a failure summary including one or more of counting the total number of failed locations, counting the total number of failed locations with massive failure, counting the number of failed locations with non-massive failures; counting the number of single-bit failures and the number of multi-bit failures identified associated with said column or row under test.

16. A method as defined in claim **1**, said generating a failure summary including concurrently generating two or more failure summaries and said transferring including shifting said two or more failure summaries from said circuit in parallel via respective circuit serial outputs.

17. A method as defined in claim **16**, said two or more failure summaries including a failure summary for each of two or more memories tested in parallel.

18. A method as defined in claim **16**, said two or more failure summaries including a failure summary for each of two or more sections of a memory.

19. A method as defined in claim **1**, said failure summary including failure summary fields associated with each of two or more segments of said memory and fields relating to the complete column or row.

20. A method as defined in claim **1**, said generating a failure summary including encoding selected failure information.

21. A method as defined in claim **20**, said encoding selected failure information including encoding failure counts of each of predetermined failure types when a count of a failure type exceeds a predetermined value.

22. A method as defined in claim **21**, said encoding including determining a percentage of the number of defective cells in a column or row.

23. A method as defined in claim **21**, said encoding selected failure information further including maintaining a count of the number of errors in each of two or more groups of adjacent cells in said column or row and including each said count in said failure summary.

24. A method as defined in claim **20**, said encoding selected failure information including encoding failure mask data.

25. A method as defined in claim **20**, said encoding selected failure information including providing an index to identify a bit position of a memory output that failed together with a bit to indicate whether a failure mask contains more than one failing bit.

26. A method as defined in claim **1**, said generating a failure summary including, generating in parallel a separate failure summary for each of two or more groups of a predetermined number of memory outputs.

27. A method as defined in claim **26**, each said separate failure summary including a first field for identifying a failing group, a second field for failure mask data of said failing group, and a third field for indicating whether one or more other groups contain failures.

28. A method as defined in claim **27**, said failure summary including a flag field associated with each group for indicating whether an adjacent group is also defective.

29. A method as defined in claim **1**, said failure summary including a flag field associated with a column or row address field of a failing cell for indicating whether an adjacent cell is also defective.

30. A method as defined in claim **1**, said selectively generating a failure summary further including generating a column failure summary when said algorithm is in column access mode, generating a row failure summary when said algorithm is in row access mode, and, following completion of a test phase, generating a phase failure summary.

31. A method as defined in claim **1**, said selectively generating a failure summary including generating a failure summary only when said algorithm is in a column access mode.

32. A method of collecting memory failure information in real time while performing a test of memory embedded in a circuit for memory test phases that use a column or a row access mode, comprising, for each memory column or row under test:

testing each memory location of said column or row according to a memory test algorithm under control of a first clock;

generating on-circuit a failure summary while testing said column or row, said generating a failure summary including, for each detected failure:

determining whether said detected failure is a massive failure or a non-massive failure; and, if said detected failure is a non-massive failure:

classifying said detected failure according to predetermined failure types; and

updating a failure mask register with results of comparisons of memory outputs and expected memory outputs;

incrementing a count of each detected failure type; and

storing the row or column address of the first and last failures in said column or row, respectively;

upon completion of testing of said column or row, selecting a failure summary data depending upon whether a column or row was tested; and

transferring said failure summary from said circuit under control of said second clock concurrently with testing of the next column or row in sequence.

33. A method as defined in claim **32**, said failure summary having a bit length equal to or less than the time required to test a column or row of said memory divided by the period of a second clock.

34. A method as defined in claim **32**, further including initiating said transferring said failure summary at the end of testing said column or row or at the end of transferring of an immediately preceding failure summary.

35. A method as defined in claim **34**, further including delaying testing of the second next column or row in sequence until said failure summary has been completely transferred.

36. A method as defined in claim **32**, further including performing said transferring said failure summary during a transfer time substantially equal to the time required to test a corresponding row or column.

37. A method as defined in claim **32**, further including performing said transferring said failure summary during a transfer time equal to or less than the time required to test a corresponding row or column.

38. A method as defined in claim **32**, each said failure summary comprising a combination of one or more of a column or row failure address, one or more failure counts, and failure mask data.

39. A method as defined in claim **32**, said selectively generating a failure summary further including generating a column failure summary when said algorithm is in column access mode, generating a row failure summary when said algorithm is in row access mode, and, following completion of a test phase, generating a phase failure summary.

40. A method as defined in claim **32**, said selectively generating a failure summary including generating a failure summary only when said algorithm is in a column access mode.

41. A memory test controller for testing memory in a circuit, comprising:

means for testing each memory location of a column or row of said memory according to a test algorithm under control of a first clock;

means for generating a failure summary while testing a column or row of said memory; and

means for transferring said failure summary from said circuit via a circuit output under control of a second clock while testing the next column or row, if any, of a memory under test.

42. A memory test controller as defined in claim **41**, said means for generating a failure summary including a transfer register for storing failure summary data.

43. A memory test controller as defined in claim **42**, said transfer register having a maximum bit length equal to or less than the time required to test a column or row of said memory divided by the period of said second clock.

44. A memory test controller as defined in claim **42**, said means for generating a failure summary including means responsive to phase input signals and memory access mode signals for selecting failure data to insert into said failure summary.

45. A memory test controller as defined in claim **41**, further including failure type identification means responsive to a failure mask for classifying detected failures according to predetermined failure types.

46. A memory test controller as defined in claim **45**, said means for generating a failure summary including a counter means for counting detected failures of each of said predetermined failure types.

47. A memory test controller as defined in claim **41**, said means for generating a failure summary including failure address registers for storing the row or column address of a first and of a last failure, if any, of a column or row under test.

48. A memory test controller as defined in claim **41**, further including a failure mask register for storing results of comparisons of memory data outputs against expected data outputs.

49. A memory test controller as defined in claim **41**, further including means for encoding selected failure summary information.

50. A memory test controller as defined in claim **49**, said means for encoding selected failure information including means for encoding failure counts of each of predetermined failure types when a count of a failure type exceeds a predetermined value.

51. A memory test controller as defined in claim **50**, said means for encoding including further including means for determining a percentage of the number of defective cells in a column or row.

52. A memory test controller as defined in claim **50**, said means for encoding selected failure summary information further including means for maintaining a count of the number of errors in each of two or more groups of adjacent cells in said column or row and including each said count in said failure summary.

53. A memory test controller as defined in claim **49**, said means for encoding selected failure summary information including means for encoding failure mask data.

54. A memory test controller as defined in claim **49**, said means for encoding selected failure summary information including means for providing an index to identify a bit position of a memory output that failed and a bit to indicate whether a failure mask contains more than one failing bit.

55. A memory test controller as defined in claim **41**, said means for generating a failure summary including:

a failure type identification circuit for determining a failure type of each detected failure;

a failure type counter for each of said predetermined failure type;

a failure mask register for storing results of comparisons between each memory output and corresponding expected memory outputs;

failure address registers for storing the row or column address of each of first and last failure in a column or row;

a failure summary selection circuit for determining the content of said failure summary, and

a failure summary transfer register for holding said failure summary and;

a circuit for controlling shifting of failure data into and out of said transfer register.

56. A memory test controller for testing memory in a circuit, comprising:

means for testing each memory location of a column or row of a memory under test according to a test algorithm under control of a first clock;

a failure summary generator for generating a failure summary while testing a column or row of said memory, including:

failure type identification means responsive to a failure mask for classifying detected failures according to predetermined failure types;

counter means responsive to outputs of said failure type identification means for counting failures of each said predetermined types;

failure address registers for storing the row or column address of first and last detected failures in a column or row under test; and

a failure mask register for storing a failure mask containing results of comparisons of memory data outputs against expected data outputs;

means responsive to phase input signals and memory access mode signals for selecting failure data to insert into said failure summary

a failure summary transfer register having a bit length equal to or less than the time required to test a column or row of said memory divided by the period of said second clock; and

means for transferring said failure summary from said circuit via a circuit serial output under control of a second clock while testing the next column or row, if any, of a memory under test.